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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/644,730	08/21/2003	Shinsaku Sckido	60188-630	6195

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Jack Q. Lever, Jr.
McDERMOTT, WILL & EMERY
600 Thirteenth Street, N.W.
Washington, DC 20005-3096

EXAMINER	
PIERRE LOUIS, ANDRE	
ART UNIT	**PAPER NUMBER**
2123	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	04/09/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/644,730	SEKIDO ET AL.	
	Examiner	Art Unit	
	Andre Pierre-Louis	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 January 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *12-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *12-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. The amendment filed on 01/18/2007 has been received and fully considered.

2. Claims 1-11 are cancelled; and now new claims 12-21 are presented for examination.

Response to Arguments

3. Applicant's arguments filed 01/18/2007 have been entered and fully considered, but are moot in view of the new ground of rejection below.

3.1 Regarding the rejection under 35 USC 101, the examiner maintains the rejection, as applied to the new claims below, as the Applicants fail to overcome the rejection.

Claim Rejections - 35 USC § 101

3. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

The claimed invention as a whole must accomplish a practical application. That is, it must produce a "useful, concrete and tangible result." State Street, 149 F.3d at 1373, 47USPQ2d at 1601-02. The purpose of this requirement is to limit patent protection to inventions that possess a certain level of "real world" value, as opposed to subject matter that represents nothing more than an idea or concept, or is simply a starting point for future investigation or research (Brenner v. Manson, 383 U.S. 519, 528-36, 148 USPQ 689, 693-96); In re Ziegler, 992, F.2d 1197, 1200-03, 26 USPQ2d 1600, 1603-06 (Fed. Cir. 1993)). Accordingly, a complete disclosure should contain some indication of the practical application for the claimed invention, i.e., why the applicant believes the claimed invention is useful. However, the mere fact that the claim may satisfy the utility requirement of 35 U.S.C. 101 does not mean that a useful result is achieved under the practical application requirement. The claimed invention as a whole must produce a

"useful, concrete and tangible" result to have a practical application.

3.0 Claims 12-21 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. While canceling the previously presented claims, the new claims, as presented, still do not produce a useful, tangible, concrete result. The Examiner further notes that that while the claims recite a plurality of method steps for simulating a circuit, the claims do not provides the end results of having these steps performed. ***See MPEP 2106 [R2]***

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

4.0 Claims 12-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Smith et al. (USPG_PUB No. 20030229875), in view of Shimizu et al. (U.S. PG_PUB No. 2001/0008293).

4.1 In considering the independent claim 12, Smith et al. substantially teaches a circuit simulation method comprising the steps of (a) recognizing, from mask layout data for an

integrated circuit, the shape of a first transistor portion which is provided in the integrated circuit *(fig.22-25, para 0042,0144,0180,0189)*; (b) obtaining transistor size data and transistor model recognition data of the first transistor portion based on a result of the step of recognizing the shape of the first transistor portion *(fig.24-25, para 0042,114,180,189)*; (c) obtaining device measurement data by measuring an electrical characteristic of a device for measurement in which transistors each having a different stress are provided *(fig.7 (33-2), fig.15-16)*; (d) recognizing, from the device measurement data, the shape of a second transistor portion which is provided in the device for measurement *(fig.22-25, para 180,189)*; (e) extracting parameters based on a result of the step of recognizing the shape of the second transistor portion and converting the device measurement data into parameters having model parameter groups according to the stress *(fig.7 (31), 15-16)*; (f) inputting as a netlist the transistor size data and the transistor model recognition data in a circuit simulator and inputting in the circuit simulator the parameters having the model parameter groups according to the stress *(fig.7 (34,37), para 134,175,203)*; and
(g) selecting, using the circuit simulator, a parameter suitable for each of the transistors provided in the integrated circuit from among the parameters having the model parameter groups according to the stress to carry out a circuit simulation in consideration of a stress applied to each of the transistors *(fig.9 (31.5-31.6), fig.16 (34-1-3), para 203,235,262)*. Smith et al. does not clearly teach the term stress to the device. Shimizu et al. substantially teaches a method for MIS transistor manufacturing including applying stress to the device (*see title, para 0034-0036*). Smith et al. and Shimizu et al. are analogous art because they are from the same field of endeavor and that the method teaches by Shimizu et al. is similar to that of Smith et al. Therefore it would have been obvious to one ordinary skilled in the art at the time of the applicant's

invention to combine the MIS transistor manufacturing method of Shimizu et al. with the circuit fabrication method of smith et al. because Shimizu et al. teaches the advantage of using the sidewall spacer to obtain improvement in hot electron resistance (*para 0035*).

4.2 Regarding claim 13, the combined teachings of Smith et al. and Shimizu et al. substantially teach that the step (a) recognizes a width of a source/drain region extending, at one side, from one end of a gate electrode to an isolation region and a width of the isolation region, as the step of recognizing the shape of the first transistor portion *(see Shimizu et al. fig.1-3, para 0030-0032); also see Smith et al. fig.7*).

4.3 As per claim 14, the combined teachings of Smith et al. and Shimizu et al. substantially teach that the step (d) recognizes a width of a source/drain region extending, at one side, from one end of a gate electrode to an isolation region and a width of the isolation region, as the step of recognizing the shape of the second transistor portion (*see Shimizu et al. fig.1-3, para 0030-0032); also see Smith et al. fig.22-25).*

4.4 With regards to claim 15, the combined teachings of Smith et al. and Shimizu et al. substantially teach that in the step (b), the transistor size data includes a transistor size comprising a gate length and a gate width *(see Shimizu et al. fig.13, para 0009, 0034); also see Smith et al. fig.22-25).*

4.5 Regarding claim 16, the combined teachings of Smith et al. and Shimizu et al. substantially teach that in the step (g), a most suitable model parameter is selected from among the model parameter groups in accordance with the stress to carry out the circuit simulation, even in a situation where transistors have a same size *(see Smith (fig.9 (31.5-31.6), fig.16 (34-1-3), para 203,235,262); also see Shimizu et al. para 0034-0036).*

4.6 As per claim 17, the combined teachings of Smith et al. and Shimizu et al. substantially teach that the transistors are each formed by a MIS transistor comprising a gate electrode, a gate insulating film, an active region and an isolation insulating film surrounding the active region *(see Shimizu et al. title, abstract, fig.1-3, para 0030-0036)*; wherein the step (c) at least includes a step of measuring items each serving as an index of the stress applied from the isolation insulating film to each of the MIS transistors *(see Shimizu et al. fig.1-3, para 0030-0036)*; and wherein the items, each serving as an index of the stress applied to each of the MIS transistors, include at least one of a position of the gate electrode in the active region, a size of the active region, and a width of the isolation insulating film *(see Shimizu et al. fig.1-3, para 0030-0036)*.

4.7 With regards to claim 18, the combined teachings of Smith et al. and Shimizu et al. substantially teach that the items, each serving as an index of the stress applied to the MIS transistors, further include at least one of a depth of the active region, a method for forming the isolation insulating film, a depth of the isolation insulating film, a material for use in forming the isolation insulating film, a size of the gate insulating film, and a material for use in forming the gate insulating film *(see Shimizu et al. title, abstract, fig.1-4, para 0030-0036); also see Smith et al. fig.5-7)*.

4.8 As per claim 19, the combined teachings of Smith et al. and Shimizu et al. substantially teach that in the step (e), model parameter groups including additional models are prepared *(see Smith et al. fig.7, para 134,175,203); also see Shimizu et al. fig.1-3, para 0030-0036);* wherein in the step (f), the parameters having the model parameter groups including the additional models are input to the circuit simulator *(see Smith et al. fig.7, para 134,175,203);*

also see Shimizu et al. fig.1-3, para 0030-0036); and wherein in the step (g), a correction is made using the additional models when selecting a parameter suitable for each of the transistors provided in the integrated circuit *(see Smith et al. fig.7, para 134,175,203); also see Shimizu et al. fig.1-3, para 0030-0036).*

4.9 Regarding claim 20, the combined teachings of Smith et al. and Shimizu et al. substantially teach that after the steps (a) and (d) and prior to the step (g), the step of preparing a reference table including pieces of information for associating each of the transistors provided in the integrated circuit with the parameter that should be assigned to the each of the transistors based on the results of the step of recognizing the shape of the first transistor portion and the step of recognizing the shape of the second transistor portion, and the step of inputting the reference table to the circuit simulator, and wherein in the step (g), the selection of the parameter suitable for each of the transistors provided in the integrated circuit is automatically carried out using the reference table *(see Smith et al. fig.11,16-17, para 175-178); also see Shimizu et al. fig.1-3, para 0030-0036).*

4.10 With regards to claims 21, the combined teachings of Smith et al. and Shimizu et al. substantially teach that the reference table is used to associate each of the transistors provided in the integrated circuit with a plurality of weighted parameters *(see Smith et al. fig.11, 16-17, para 175-178); also see Shimizu et al. fig.1-3, para 0030-0036).*

5.0 Claim 12 is further rejected under 35 U.S.C. 103(a) as being unpatentable over Smith et al. (USPG_PUB No. 20030229875), in view of Yonezawa et al. (U.S. Patent No. 6,795,802).

5.1 In considering the independent claim 12, Smith et al. substantially teaches a circuit simulation method comprising the steps of (a) recognizing, from mask layout data for an

integrated circuit, the shape of a first transistor portion which is provided in the integrated circuit *(fig.22-25, para 0042,0144,0180,0189)*; (b) obtaining transistor size data and transistor model recognition data of the first transistor portion based on a result of the step of recognizing the shape of the first transistor portion *(fig.24-25, para 0042,114,180,189)*; (c) obtaining device measurement data by measuring an electrical characteristic of a device for measurement in which transistors each having a different stress are provided *(fig.7 (33-2), fig.15-16)*; (d) recognizing, from the device measurement data, the shape of a second transistor portion which is provided in the device for measurement *(fig.22-25, para 180,189)*; (e) extracting parameters based on a result of the step of recognizing the shape of the second transistor portion and converting the device measurement data into parameters having model parameter groups according to the stress *(fig.7 (31), 15-16)*; (f) inputting as a netlist the transistor size data and the transistor model recognition data in a circuit simulator and inputting in the circuit simulator the parameters having the model parameter groups according to the stress *(fig.7 (34,37), para 134,175,203)*; and (g) selecting, using the circuit simulator, a parameter suitable for each of the transistors provided in the integrated circuit from among the parameters having the model parameter groups according to the stress to carry out a circuit simulation in consideration of a stress applied to each of the transistors *(fig.9 (31.5-31.6), fig.16 (34-1-3), para 203,235,262)*. Smith et al. does not clearly teach applied stress to the device. Yonezawa et al. teaches applied stress and further teaches a stress calculation unit *(fig.5 (111b), col.7 line 43-col.10 line 65; also col.12 line 61-col.14 line 49)*. It would have been obvious to one ordinary skilled in the art at the time of the applicant's invention to combine the stress calculation of Yonezawa et al. in the circuit simulation method of

Smith et al. for the purpose of calculating and analyzing the stress applied to the device. Yonezawa et al. further teaches the improvement of processing efficiency *(col.12 lines 25-45)*.

Conclusion

6. Claims 12-21 are rejected and Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andre Pierre-Louis whose telephone number is 571-272-8636. The examiner can normally be reached on Mon-Fri, 8:00AM-4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Paul L. Rodriguez can be reached on 571-272-3753. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

March 23, 2007
APL

3/30/07

PAUL RODRIGUEZ
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100